

Kindly replace the paragraph beginning on page 13, line 26 with the following:

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-- As mentioned above, according to Embodiment 4, since the connection is done by both the common contact hole 60 and diffused layer 20, the variation of resistance value may be suppressed. --

IN THE CLAIMS:

Please replace claims 4, 6, 7, 10, 11 and 13 and add new claim 17 as follows:

4. (Amended) A semiconductor device, comprising:

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a gate electrode formed on a substrate through a gate insulating film;

a diffused layer formed on the substrate;

a wiring layer formed above the gate electrode; and

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a contact formed within a contact hole between the wiring layer and the substrate,

which connects the wiring layer to the diffused layer and the gate electrode,

wherein the diffused layer has first and second portions formed opposite to each other across the portion of the substrate existing under the gate electrode and having a first conduction type, each having a second conduction type different from the first conduction type of the portion of the substrate; and a third portion that connects the first portion to the second portion.

B7 D17
6. (Amended) A semiconductor device according to claim 4, comprising:

another diffused layer formed on the substrate; and

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an isolation area formed between the diffused layer and said other diffused layer,
which separates the diffused layer and the other diffused layer, wherein the contact is
connected further to the other diffused layer.

7. (Amended) A semiconductor device according to claim 1, comprising a
SRAM cell, wherein the wiring layer is connected to a memory node of the SRAM cell.

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10. (Amended) A semiconductor device according to claim 1, comprising
another gate electrode formed on the substrate through another gate insulating film, and a
transistor for composing a semiconductor IC therein, wherein the relative dielectric
constant of the gate insulating film is higher than the one of said another gate insulating
film.

11. (Amended) A semiconductor device according to claim 1, comprising a
source area and a drain area formed opposed to each other across a channel portion of the
substrate existing under the gate electrode, and a transistor for composing a semiconductor
IC therein, wherein the impurity concentrations of the first diffused layer and the second
diffused layer are higher than the ones of the source and the drain areas.

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13. (Twice Amended) A semiconductor device according to claim 4,
comprising a SRAM cell, wherein the wiring layer is connected to a memory node of the
SRAM cell.

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17. (New) A semiconductor device, comprising:

- a gate electrode formed on a substrate through a gate insulation film lying therebetween;
- first and second diffused layers formed opposite to each other across the portion of the substrate existing under the gate electrode and having a first conduction type, each having a second conduction type different from the first conduction type of the portion;
- a wiring layer formed above the gate electrode; and
- a contact formed within a contact hole between the wiring layer and the substrate, which electrically connects the wiring layer to the first diffused layer and the gate electrode.